IN THE CLAIMS:

Please amend claims 1, 8 and 15 as follows:

1. (Currently Amended) A disk array device comprising:

a plurality of hard disk drives;

a plurality of channel control units for performing data transfer and reception between these units and [[an]] a plurality of information processing apparatuses being communicably connected thereto through a storage area network;

a plurality of disk control units for performing data transfer and reception between these units and said plurality of hard disk drives as communicably connected thereto;

a CPU for performing control of said plurality of channel control units and said plurality of disk control units;

a cache memory for storage of data being transferred and received between said channel control units and said disk control units; and

a data transfer integrated circuit communicably connected via more than one bus to said channel control units, said disk control units and said CPU and also connected via a plurality of data buses to said cache memory, wherein

said data transfer integrated circuit is responsive to an access request to said cache memory from one of said channel control units, said disk control units and said CPU, for providing access to said cache memory using more than one of said data [[bases]] buses, a number of which is determined in accordance with a transfer data length being set in the access request.

2. (Original) The disk array device according to claim 1, wherein said bus is a PCI bus with a width of 64 bits and wherein said transfer data length of said access request is set to upper 32 bits in an address phase of said PCI bus.

3. (Original) The disk array device according to claim 1, wherein

said data buses are two data buses, and

said data transfer integrated circuit uses said two data buses to provide access to said cache memory when the transfer data length being set in the access request is longer than a predefined reference data length and, when the transfer data length set in the access request is shorter than said reference data length, uses one of said data buses to get access to said cache memory.

4. (Original) The disk array device according to claim 3, wherein

said cache memory is two physically separate cache memories, and

a respective one of said two cache memories is communicably connected via said data buses to said data transfer integrated circuit.

5. (Original) The disk array device according to claim 3, wherein

said data transfer integrated circuit includes a priority adding unit for adding, when receiving access requests to said cache memory from a plurality of ones of said channel control units or said disk control units or said CPU, an order of priority to the plurality of access requests, and

said data transfer integrated circuit uses said two data buses to provide access to said cache memory when a transfer data length being set in one of said access requests with the highest order of priority is longer than said reference data length and, when transfer data lengths being set in said access request with the highest order of priority and an access request with the second highest order of priority are shorter than said reference data length, uses one of said data buses for each to thereby get access to said cache memory.

6. (Original) The disk array device according to claim 5, wherein in case the transfer data lengths being set in said access request with the highest order of priority and said access request with the second highest order of priority are shorter than said reference

data length, when both of said two data buses are out of use, said data transfer integrated circuit allocates one of said data buses to each of the two access requests and then performs access to said cache memory in a parallel way.

7. (Original) The disk array device according to claim 5, wherein in case the transfer data length being set in said access request with the highest order of priority is longer than said reference data length, when any one of said two data buses is in use, said data transfer integrated circuit allocates a remaining one of said data buses which is out of use with respect to the access request and then performs access to said cache memory.

8. (Currently Amended) A control method of a disk array device arranged to include:

a plurality of channel control units for performing data transfer and reception between these units and [[an]] a plurality of information processing apparatuses being communicably connected thereto through a storage area network;

a plurality of disk control units for performing data transfer and reception between these units and a plurality of hard disk drives as communicably connected thereto;

a CPU for performing control of said plurality of channel control units and said plurality of disk control units;

a cache memory for storage of data being transferred and received between said channel control units and said disk control units; and

a data transfer integrated circuit communicably connected via more than one bus to said channel control units, said disk control units and said CPU and also connected via a plurality of data buses to said cache memory, wherein

an operation in said data transfer integrated circuit includes the steps of:

receiving an access request to said cache memory from any one of said channel control units, said disk control units and said CPU;

selecting certain one or ones of said data [[bases]] buses, a number of which is determined in accordance with a transfer data length being set in the access request; and

using the selected data bus to thereby provide access to said cache memory.

9. (Original) The disk array device control method according to claim 8, wherein said bus is a PCI bus with a width of 64 bits and wherein said step of selecting the data buses selects a specified number of data buses, which number is determinable in accordance with said transfer data length of said access request being set at upper 32 bits in an address phase of said PCI bus.

10. (Original) The disk array device control method according to claim 8, wherein said data buses are two data buses, and

said step of selecting the data buses includes one of the steps of:

selecting said two data buses when the transfer data length being set in the access request is longer than a predefined reference data length; and

selecting one of said data buses when the transfer data length as set in the access request is shorter than said reference data length.

11. (Original) The disk array device control method according to claim 10, wherein said cache memory is two physically separate cache memories, and

a respective one of said two cache memories is communicably connected via said data buses to said data transfer integrated circuit.

12. (Original) The disk array device control method according to claim 10, wherein said data transfer integrated circuit has a step of adding, when receiving access requests to said cache memory from a plurality of ones of said channel control units or said disk control units or said CPU, an order of priority to the plurality of access requests, and

said step of selecting the data buses includes one of the steps of:

selecting said two data buses when a transfer data length being set in one of said access requests with the highest order of priority is longer than said reference data length, and

when transfer data lengths being set in said access request with the highest order of priority and an access request with the second highest order of priority are shorter than said reference data length, selecting one of said data buses for each.

13. (Original) The disk array device control method according to claim 12, wherein in an event that the transfer data lengths being set in said access request with the highest order of priority and said access request with the second highest order of priority are shorter than said reference data length, when both of said two data buses are out of use, said step of selecting the data buses selects one of said data buses to each of the two access requests.

14. (Original) The disk array device control method according to claim 12, wherein in case the transfer data length being set in said access request with the highest order of priority is longer than said reference data length, when any one of said two data buses is in use, said step of selecting the data buses selects a remaining one of said data buses which is out of use with respect to the access request.

15. (Currently Amended) A disk array device comprising:

a first controller and a second controller each including,

a plurality of channel control units for performing data transfer and reception between these units and [[an]] a plurality of information processing apparatuses being communicably connected thereto through a storage area network;

a plurality of disk control units for performing data transfer and reception between these units and said plurality of hard disk drives as communicably connected

thereto;

a CPU for performing control of said plurality of channel control units and said plurality of disk control units;

a cache memory for storage of data being transferred and received between said channel control units and said disk control units; and

a data transfer integrated circuit communicably connected via more than one bus to said channel control units, said disk control units and said CPU and also connected via a plurality of data buses to said cache memory; and

said plurality of hard disk drives, wherein

said data transfer integrated circuit of said first controller and the data transfer integrated circuit of said second controller are communicably connected together,

said data transfer integrated circuit of said first controller transfers, when an access request to said cache memory of said second controller from any one of said channel control units, said disk control units and said CPU, an access request toward said data transfer integrated circuit of said second controller, which request sets therein an access type indicative of whether the access request is from any one of said channel control units and said disk control units or from said CPU, and

said data transfer integrated circuit of said second controller is responsive to said access request from said data transfer integrated circuit of said first controller, for providing access to said cache memory of said second controller by use of a specified number of ones of said data buses, which number is determinable in accordance with said access type being set in the access request.

16. (Original) The disk array device according to claim 15, wherein said data buses of said second controller are two data buses, and

said data transfer integrated circuit of said second controller uses said two data buses to get access to said cache memory when said access type being set in said access request as received from said data transfer integrated circuit of said first

controller is an access request from any one of said channel control units and said disk control units, and, when said access type being set in said access request is an access request from said CPU, uses a single one of said data buses to get access to said cache memory.